REMARKS

These remarks are in response to the Office Action dated May 20, 2010, which has a shortened statutory period for response set to expire August 20, 2010. No extension of time is required.

Claims

Claims 1-26, 29-30, 34-36, and 40-60 are pending in the above-identified application. Claims 1-26, 29-30, 34-36, and 40-60 are rejected over prior art. Claims 1, 14, 19, 23, 42-43, 50, 53, and 56-59 are amended, and Claims 27-28, 31-33, and 37-39 were previously canceled. Claims 2-13, 15-18, 20-22, 24-26, 29-30, 34-36, 40-41, 44-49, 51-52, 54-55, and 60 remain as filed or as previously presented. Reconsideration is requested.

Rejections Under 35 U.S.C. § 112

Claims 1-26, 29-30, 34-36, and 40-60 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The Examiner writes (in part):

> … The independent claims have been amended to state "intercommunication between each pair of connected computers is carried out through the processors of each pair of connected computer" or similarly. Applicants add this in an attempt to distinguish their invention over the prior art, specifically Fujii. The issue is that the specification fails to mention pairs or communication between each pairs; while the specification and drawings suggest a connection, nothing is specifically said about between pairs. Thus the newly added limitations are not supported by the specification.

Applicant respectfully traverses.

MPEP 2163.02 provides the standard for determining compliance with the Written Description requirement:

> … The courts have described the essential question to be addressed in a description requirement issue in a variety of ways. An objective standard for determining compliance with the written description requirement is, "does the description clearly allow

> persons of ordinary skill in the art to recognize that he or she invented what is claimed." *In re Gosteli*, 872 F.2d 1008, 1012, 10 USPQ2d 1614, 1618 (Fed. Cir. 1989). Under *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991), to satisfy the written description requirement, an applicant must convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention, and that the invention, in that context, is whatever is now claimed.

Claim 1 was previously amended to include the limitation "intercommunication between each pair of connected computers is carried out through the processors of each pair of connected computers." Applicant's previous amendment indicated support for this limitation at least in Fig. 2 and at page 5, lines 6-12; and page 7, lines 9-14 of Applicant's original disclosure. In view of these passages, and the additional citations below, Applicant respectfully avers that Claim 1 satisfies the Written Description requirement of 35 U.S.C. § 112, first paragraph.

Fig. 1 shows a computer array 10 that includes a plurality of computers 12 that are interconnected via dedicated data lines 16. Specifically, a neighboring pair of computers 12 is interconnected via the data line 16 that is dedicated between that neighboring pair of computers 12 (page 4, lines 16-22; page 5, lines 2-12). Fig. 2 shows a diagrammatic view of one of the computers 12 of the array 10. The computer 12 includes a processor 28, a ROM 30, and a RAM 32. As shown in Fig. 2, the data lines 16 are coupled to the processor 28 of the computer 12 (page 6, line 29 to page 7, line 2).

The specification discusses intercommunication between pairs of connected computers at several locations. For example, page 5, lines 6-12 indicates that a signal must "hop" from computer to computer. Page 7, lines 9-14 also indicate that "hops" are required in a 5-by-5 computer array to "relay data from one of the exterior computers 12, through others of the computers 12, to an interior computer 12." Thus, the specification clearly indicates that intercommunication is carried out between "pairs" of connected computers. Additionally, it is clear from Figs. 1 and 2 that this intercommunication between computers 12 occurs via the data lines 16.

Applicant's original specification also provides that such intercommunication is carried out by the execution of the instructions by the processors of each pair of connected computers, as claimed. As indicated above, page 7, lines 9-14 provide that data is relayed **through** the computers 12. Moreover, Fig. 2 shows that the data lines 16 are coupled to the processor 28 of the computer 12. Accordingly, the processor 28 must play a role in carrying out such intercommunication. Moreover, page 9, lines 17-30 of Applicant's specification provides several times that the computers 12 are "programmed" to communicate:

> Computers 12o and 12p are configured and **programmed to sample** and process received RF signals (analog to digital conversion) and the computer 12n is configured and **programmed to provide** reference frequencies for frequency down conversion prior to sampling (digital to analog conversion). Computer 12w and 12x are configured and programmed to decode the forward error corrected ("FEC") bit stream from the GPS signal. The FEC used in GPS signals will be familiar to on skilled in the art of GPS receivers.
>
> Computer 12y and 12h are optionally used for decrypting aspects of the GPS bit stream after reception demodulation. Note that the use of computers 12y and 12h as described is optional because encryption and decryption will not normally be required in a GPS receiver. Although some parts of a GPS signal are encrypted, a commercial receiver will generally not have access to those. However, encryption will be required in a military version of a GPS receiver. Computer 12l is configured and **programmed to communicate** with additional computer array(s) 10, as may be necessary or desirable. (Emphasis added).

Because the computers 12 are "programmed" to communicate, it should be clearly understood that the execution of the instructions by the processor 28 will carry out communication when that processor 28 executes its programming.

For the above reasons, Applicant respectfully avers that previously-presented Claim 1 satisfies the Written Description requirement of 35 U.S.C. § 112, first paragraph because the specification clearly indicates, to a person of ordinary skill in the art, that the inventor was in possession of the claimed invention when the application was filed. Claims 14, 19, 23, 42-43, 50, 53, and 56-59 were previously amended to include limitations similar to Claim 1. Therefore, each of Claims 14, 19, 23, 42-43, 50, 53, and 56-59 satisfies the written description requirement for the same reasons as Claim 1. Each of Claims 2-13, 15-18, 20-22, 24-26, 29-30, 34-36, 40-41,

44-49, 51-52, 54-55, and 60 depend, either directly or indirectly, from one of independent Claims 1, 14, 19, 23, 43, 50, and 53 and, therefore, satisfies the Written Description requirement for the same reasons as Claims 1, 14, 19, 23, 43, 50, and 53.

For the above reasons, Applicant respectfully requests reconsideration and withdrawal of the rejections under 35 U.S.C. § 112, first paragraph.

Rejections Under 35 U.S.C. § 103

Claims 1-4, 6-14, 16-21, 23-26, 30, 34, 40-42, 45-55, and 57-60 are rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Publication No. 2004/0107332 (Fujii et al.) in view of U.S. Patent No. 6,023,753 (Pechanek1) and further in view of U.S. Patent No. 6,507,947 (Schreiber et al.).

Claims 1-4, 6-13, 30, 34, 40-41, 45-49, and 60:

Regarding Claim 1, the Examiner writes (in part):

> Regarding claim 1, Fujii discloses a computer array, comprising: a plurality of computers and a plurality of data paths connecting the computers, the data paths being dedicated for communication between associated pairs of computers ([0072]); and wherein at least some of the computers are assigned a [task different] from that assigned to the other computers ([0008]); and intercommunication between each pair of connected computers is carried out through the processors of each pair of connected computers (FIG. 12).
>
> Fujii fails to disclose that the computers are integrated on a unitary substrate.
>
> Pechanek1 discloses a plurality of computers on an array on an integrated circuit (col 2 lines 24-27)
>
> …
>
> Fujii fails to disclose a plurality of computers including read-only memory and random access memory for holding instructions and data.
>
> Schreiber discloses the limitations that Fujii lacks.
>
> …
>
> ([ ] changed by Applicant)

Applicant respectfully traverses.

Principles of Law:

M.P.E.P. § 2142 provides that the examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness. If the examiner does not provide a prima facie case of obviousness, then the rejection is improper, and the applicant is under no obligation to submit evidence of non-obviousness.

In *In re Wada and Murphy*, Appeal 2007-3733, Decision on Appeal dated January 14, 2008, pages 7 and 8, the BPAI expressly indicated that, to establish a prima facie case of obviousness, the cited prior art must teach or suggest all the limitations of the claimed invention:

> When determining whether a claim is obvious, an examiner must make "a searching comparison of the claimed invention – *including all its limitations* – with the teaching of the prior art." *In re Ochiai*, 71 F.3d 1565, 1572 (Fed. Cir. 1995) (emphasis added). Thus, "obviousness requires a suggestion of all limitations in a claim." *CFMT, Inc. v. Yieldup Intern. Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003) (citing *In re Royka*, 490 F.2d 981, 985 (CCPA 1974)). Moreover, as the Supreme Court recently stated, "*there must be some articulated reasoning* with some rational underpinning to support the legal conclusion of obviousness." *KSR Int'l v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (emphasis added)).
>
> ...
>
> It is well settled that the "Patent and Trademark Office (PTO) must consider all claim limitations when determining patentability of an invention over the prior art." *In re Lowry*, 32 F.3d 1579, 1582 (Fed. Cir. 1994).
>
> (all emphasis is BPAI's emphasis)

However, a claimed invention composed of several elements is not proved obvious by merely demonstrating that each of its elements was, independently, known in the prior art. *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007). Rather, the examiner must identify a reason that would have prompted a person of ordinary skill in the art to combine the elements in the way the claimed invention does. *Id.* Specifically, as indicated above, there must be some articulated reasoning with a rational underpinning to support a conclusion of obviousness; a conclusory statement will not suffice. *Id.*, quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006).

Argument:

Fujii et al. discloses a single array-type processor 100 that includes a plurality of processor elements 102 that are controlled by a plurality of state control units 101 (*Fujii et al.*, paragraph [0042]). Each of the state control units 101 is connected to the processor elements 102 in an associated element area 105 (*Id.,* paragraph [0043]). The state control units 101 control the state transitions of the processor elements 102 causing processor elements 102 to process data (*Id.*, paragraph [0048]).

Claim 1 recites (in part) "a plurality of data paths connecting the computers, the data paths being dedicated for communication between associated pairs of the computers". Applicant respectfully avers that Fujii et al. does not disclose this element of Claim 1. Rather, Fujii et al. discloses that the switch elements 108 control the connection relationship between different processor elements 102 via the data busses 109 and 110 ([0009], [0049], [0061], and [0062]; FIG. 4A). Indeed, as shown in FIG. 4A, mb-busses 109 and nb-busses 110 are disposed between switch elements 108 and are <u>not dedicated</u> for communication between associated pairs of processor elements 102. Instead, the mb-busses 109 and nb-busses 110 are each used by more than two of the switch elements 108.

Applicant also notes that the rejection of Claim 1 appears to confuse different elements of Fujii et al. Specifically, the rejection cites paragraphs [0008] and [0072] and Fig. 12. Paragraph [0008] discusses the processor elements and switch elements, such as processor elements 102 and switch elements 108 shown in Figs. 4 and 5. However, Fig. 12 shows interconnections between state control units 101, which are <u>not</u> the processor elements 102. Paragraph [0072] of the cited reference also describes the interconnections of the state control units 101. Applicant is trying to respond fully to this rejection, but is having a difficult time determining which elements of the cited reference are being characterized as meeting the specific limitations of Claim 1. Therefore, should the Examiner determine that the current claims are not allowable over the cited prior art, Applicant respectfully requests that the Examiner clarify what structures of Fujii et al. are considered to be the claimed "computers" and "data paths" so that Applicant has a fair chance to respond to the rejection.

Claim 1 also recites (in part) that "at least some of the computers are assigned a task different from that assigned to the other computers." Fujii et al. also does not appear to teach or suggest this element of Claim 1. The rejection of Claim 1 cites paragraph [0008] of Fujii et al. as providing support for this element. Paragraph [0008] of Fujii et al. provides the following:

> [0008] In this array-type processor, a multiplicity of small-scale processor elements are arranged in rows and columns together with a multiplicity of switch elements in a datapath unit, one state control unit being provided together with one of these data path units. The multiplicity of processor elements each individually execute data processing in accordance with instruction codes in which data are individually set, and switching of connection relations is controlled by a multiplicity of switch elements that are individually provided together with the processor elements.

It does not appear to Applicant that paragraph [0008] teaches the above-recited element of Claim 1. Paragraph [0008] does indicate that the processor elements "individually execute data processing in accordance with instruction codes in which **data** are individually set" (emphasis added). However, paragraph [0008] does not indicate that <u>different</u> processor elements are assigned to different tasks, that the processor elements contain different instruction codes, or that the processor elements contain different programming. Paragraph [0008] may indicate that the processor elements receive different data but that does not mean that the processor elements are assigned different tasks.

Claim 1 further recited that "intercommunication between each pair of connected computers is carried out through the processors of each pair of connected computers." As explained in Applicants' prior response, Fujii et al. does not teach or suggest this limitation of Claim 1. Rather, as shown in Fig. 4A of Fujii et al., the switch elements 108 facilitate intercommunications between the processor elements 102. The switch elements 108 can be analogized to routers, such that a communication between two processor elements 102 does not have to travel through a processor element 102. Moreover, the mb ALU 117 and the nb ALU 118 of the processor element 102 (Fig. 4B) do not appear to play a role in carrying out communication between the processor elements 102.

In response to Applicant's prior arguments, the Examiner writes:

> Applicant argues that Fujii et al. does not teach or suggest "a plurality of computers" that each includes "a processor for executing the instructions" where "intercommunication between each pair of connected computers is carried out through the processors of each pair of connected computers," as recited by amended Claim 1. Examiner disagrees. Fujii clearly illustrates a plurality of computers. The lines as shown in FIG. 12, for example, clearly show communication between the processing elements is done in a pair fashion. While a switching element is present in the invention, the communication still occurs. The claims do not exclude the use of a switch as they are left open ended.

Applicant respectfully disagrees with the Examiner's characterization of Fujii et al. As indicated above, FIG. 12 shows the state control units 101 and not the processor elements 102 (see e.g., Fujii et al., [0102]).. Moreover, as indicated above, the switch elements 108 of Fujii et al. are analogous to routers, whereby intercommunication between the processor elements 102 can be carried out by the switch elements 108 apart from the ALUs 117 and 118 of the processor elements 102.

The remaining two cited references also do not teach or suggest that "intercommunication between each pair of connected computers is carried out through the processors of each pair of connected computers," as recited by Claim 1. Pechanek1 shows in FIG. 18 that the cluster switches 86, which are located outside of the PEs, provide intercommunication between the PEs. FIG. 18 and its associated description do not indicate that processors within the PEs of Pechanek1 carry out intercommunication between the PEs. (*Pechanek1*, col. 11, lines 25-50). With regard to Schreiber et al., FIG. 24 shows an interconnect 1102 that facilitates intercommunication between the functional units (FUs) 1110-1116. Schreiber et al. does not indicate that processors within the FUs 1110-1116 carry out intercommunication between the FUs 1110-1116. (*Schreiber et al.*, col. 36, line 19 to col. 37, line 16).

In view of the above comments, Applicant believes that previously-presented Claim 1 distinguished over the cited prior art. However, in order to further clarify the distinctions between Applicant's invention and to advance prosecution of this case, Applicant has amended Claim 1 to recite that "intercommunication between one of the plurality of computers and a nearest neighbor computer connected to the one of the plurality of computers via one of the data paths is carried out by the execution of the instructions by the processors of the one of the plurality of computers and the nearest neighbor computer" and that "intercommunication between the one of the plurality of computers and a non-nearest neighbor computer must be carried out by the execution of the instructions by the processors of the one of the plurality of computers and the nearest neighbor computer." Support for these amendments to Claim 1 is provided in Applicant's original specification at least in Figs. 1-2 and page 4, lines 16-22; page 5, lines 2-12; page 6, line 29 to page 7, line 2; and page 7, lines 9-30.

Applicant believes that such amendments additionally distinguish amended Claim 1 from the cited prior art because a communication from one processor element 102 of Fujii et al. to a non-neighboring processor element 102 does not have to be carried out through a neighboring processor element 102. Regarding Pechanek1, FIG. 18 suggests that a communication from one PE to a non-neighboring PE would not have to travel through a neighboring PE first. Finally, FIG. 24 of Schreiber et al. suggests that a communication from one FU to a non-neighboring FU would not have to travel through a neighboring FU first.

Finally, Applicant notes that similar limitations to those currently amended into Claim 1 resulted in the allowance of co-pending U.S. Application No. 11/810,183, filed June 5, 2007, over the same three primary references.

For the above reasons, Applicant respectfully avers that amended Claim 1 distinguishes over the cited prior art. Claims 2-4, 6-13, 30, 34, 40-41, 45-49, and 60 depend, either directly or indirectly, from Claim 1 and are distinguished, therefore, from the cited prior art for at least the same reasons as Claim 1.

Claims 14 and 16-18:

Applicant respectfully avers that previously-presented Claim 14 distinguished over the cited prior art for the same reasons as previously-presented Claim 1. Additionally, Claim 14 is amended herein to contain limitations that are similar to amended Claim 1 and, therefore, further distinguishes over the cited prior art for the same reasons as amended Claim 1. Claims 16-18 depend directly from Claim 14 and are distinguished from the cited prior art for at least the same reasons as Claim 14.

Claims 19-21:

Applicant respectfully avers that previously-presented Claim 19 distinguished from the cited prior art for the same reasons as previously-presented Claim 1. Additionally, Claim 19 is amended herein to contain limitations that are similar to amended Claim 1 and, therefore, further distinguishes from the cited prior art for the same reasons as amended Claim 1. Claims 20-21 depend directly from Claim 19 and are distinguished from the cited prior art for at least the same reasons as Claim 19.

Claims 23-26:

Applicant respectfully avers that previously-presented Claim 23 distinguished from the cited prior art for the same reasons as previously-presented Claim 1. Additionally, Claim 23 is amended herein to contain limitations that are similar to amended Claim 1 and, therefore, further distinguishes from the cited prior art for the same reasons as amended Claim 1. Claims 24-26 depend directly from Claim 23 and are distinguished from the cited prior art for at least the same reasons as Claim 23.

Claim 42:

Applicant respectfully avers that previously-presented Claim 42 distinguished from the cited prior art for the same reasons as previously-presented Claim 1. Additionally, Claim 42 is amended herein to contain limitations that are similar to amended Claim 1 and, therefore, further distinguishes from the cited prior art for the same reasons as amended Claim 1.

Claims 50-52:

Applicant respectfully avers that previously-presented Claim 50 distinguished from the cited prior art for the same reasons as previously-presented Claim 1. Additionally, Claim 50 is amended herein to contain limitations that are similar to amended Claim 1 and, therefore, further distinguishes from the cited prior art for the same reasons as amended Claim 1. Claims 51-52 depend directly from Claim 50 and are distinguished from the cited prior art for at least the same reasons as Claim 50.

Claims 53-55:

Applicant respectfully avers that previously-presented Claim 53 distinguished from the cited prior art for the same reasons as previously-presented Claim 1. Additionally, Claim 53 is amended herein to contain limitations that are similar to amended Claim 1 and, therefore, further distinguishes from the cited prior art for the same reasons as amended Claim 1. Claims 54-55 depend directly from Claim 53 and are distinguished from the cited prior art for at least the same reasons as Claim 53.

Claims 57-59:

Applicant respectfully avers that each of previously-presented Claims 57-59 distinguished from the cited prior art for the same reasons as previously-presented Claim 1. Additionally, Claims 57-59 are each amended herein to contain limitations that are similar to amended Claim 1 and, therefore, each further distinguishes from the cited prior art for the same reasons as amended Claim 1.

Claims 5, 22, 29, 35-36, 43-44, and 56:

Claims 5, 22, 29, 35-36, 43-44, and 56 are rejected under 35 U.S.C. § 103 as being unpatentable over Fujii et al., Pechanek1, and Schreiber et al. and further in view of Common Art.

Claims 5, 29, and 35-36 depend, directly or indirectly, from amended Claim 1 and, therefore, include all the limitations of amended Claim 1. Amended Claim 1 distinguishes from the cited prior art for at least the reasons provided above. Therefore, Claims 5, 29, and 35-36 distinguish from the cited prior art for at least the same reasons as amended Claim 1.

Claim 22 depends from amended Claim 19, which distinguishes from the cited prior art for the reasons provided above. Therefore, Claim 22 also distinguishes from the cited prior art for at least the same reasons as Claim 19.

Applicant respectfully avers that previously-presented Claim 43 distinguished from the cited prior art for the same reasons as previously-presented Claim 1. Additionally, Claim 43 is amended herein to contain limitations that are similar to amended Claim 1 and, therefore, further distinguishes from the cited prior art for the same reasons as amended Claim 1. Claim 44 depends directly from Claim 43 and is distinguished from the cited prior art for at least the same reasons as Claim 43.

Applicant respectfully avers that previously-presented Claim 56 distinguished from the cited prior art for the same reasons as previously-presented Claim 1. Additionally, Claim 56 is amended herein to contain limitations that are similar to amended Claim 1 and, therefore, further distinguishes from the cited prior art for the same reasons as amended Claim 1.

Applicant also maintains the prior traversal that the "asynchronous communication" and "asynchronous operation" aspects of the present invention are officially noticed. Specifically, for the reasons provided in Applicants' prior responses, these aspects of the present invention are not "capable of such instant and unquestionable demonstration as to defy dispute," such that taking Official Notice of them would be proper under MPEP § 2144.03. Moreover, the technical line of reasoning relied upon for taking Official Notice of the above claims is insufficient. The rejection argues that "Fujii/Pechanek1/Schreiber would have been motivated to utilize the asynchronous communication in order to speed up reaction time (rather than waiting for a clock) and to make a universal clock signal unnecessary" (OA, para. 47). However, U.S. 5,410,723 (Schmidt et al.), which was cited in response to Applicant's prior traversal, requires a global clock signal (*Schmidt et al.*, col. 4, lines 11-29 and FIG. 1). Furthermore, no evidence or motivation is provided for taking the official notice of asynchronous operation.

Claim 15:

Claim 15 is rejected under 35 U.S.C. § 103 as being unpatentable over Fujii et al., Pechanek1, and Schreiber et al. and further in view of Common Art.

Claim 15 depends from amended Claim 14 and, therefore, includes all the limitations of amended Claim 14. Therefore, Claim 15 distinguishes from the cited prior art for at least the same reasons as amended Claim 14. Additionally, Applicant maintains his prior traversal that Official Notice was taken of Claim 15. To Applicant's knowledge, evidence has not been provided showing "at least one of the computers is assigned to communicate with an external flash memory," as recited by Claim 15.

Claims 31 and 33:

The Office Action indicates that Claims 31 and 33 are rejected on the same grounds as Claim 16. Applicant notes that Claims 31 and 33 were previously canceled.

For the above reasons, Applicant respectfully requests reconsideration and withdrawal of all the rejections under 35 U.S.C. § 103.

For the foregoing reasons, Applicant believes that Claims 1-26, 29-30, 34-36, and 40-60 are in condition for allowance. Should the Examiner undertake any action other than allowance of Claims 1-26, 29-30, 34-36, and 40-60, or if the Examiner has any questions or suggestions for expediting the prosecution of this application, the Examiner is requested to contact Applicant's attorney at (269) 279-8820.

Respectfully submitted,

August 20, 2010 /Larry E. Henneman, Jr./

Date:_____ _____

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CERTIFICATE OF TRANSMISSION (37 CFR 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being electronically filed with the U.S. Patent and Trademark Office on the date shown below.

August 20, 2010 /Larry E. Henneman, Jr./

Date:_____ _____

Larry E. Henneman, Jr.